Monthly Status Report • February 2010
Covering the Period 1 February through 28 February 2010

POWER MEMS DEVELOPMENT

Contract N00014-09-C-0252
Submitted in accordance with Deliverable A001 - Monthly Technical and Financial
SRI Project P19063

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ACTIVITIES AND PROGRESS

MEMS RESETTABLE CIRCUIT BREAKER (TASK 1.1) AND MEMS SWITCH FOR DC-DC VOLTAGE CONVERTERS (TASK 1.2)

Task 1.1 Contributors: Susana Stillwell, Sunny Kedia, Weidong Wang

Task 1.1 Deliverable: 10 prototype packed MEMS-based resettable circuit breakers for testing and analysis in ONR laboratories.

Task 1.2 Contributors: Sunny Kedia, Shinzo Onishi, Scott Samson

Task 1.2 Deliverable: Functional MEMS-based DC-DC converter in a vacuum package.

Task 1.1 and Task 1.2 Progress:

In January we reported that the micro-cantilevers were stuck down to the substrate after fabrication. In the past, we have not seen this failure when we used devices fabricated on silicon-on-insulator (SOI) wafers and platinum (Pt) contacts. The two mechanisms we have come up with that would lead to this failure that also include new processes that were introduced specifically for this device process flow are 1) deformation of the bond metal in the anchor region or 2) charging of the cantilever during the reactive ion etch (RIE) step. In parallel with failure analysis to determine a root cause, we continue to develop a version 2 device (VC2.0), which is not subject to those two mechanisms.

For the VC2.0 device, we are utilizing a plate and spring configuration successfully used in a previous project for an array of closely coupled optical MEMS devices to replace our single anchor "diving board" cantilever configuration used in the first version. A nominally 500 x 500 µm plate suspended on all four sides with Si springs is fabricated using the SOI wafer (Figure 1.) The electrical routing and electrostatic drive electrode are pattered on a borosilicate glass wafer (Figure 2) which is thermally matched to the SOI wafer to eliminate misalignment during wafer bonding. We designed a slightly different process flow for the VC2.0 device which follows our previous optical device process as closely as possible.

The SOI wafer processing is as follows:

- Pattern and deep reactive ion etch (DRIE) the handle silicon to define the plates, springs, anchors and bond area
- Reactive ion etch (RIE) the buried oxide (BOx) to transfer the same pattern
- Deposit, pattern and etch the silicon contact isolation spacer
- Pattern by liftoff and deposit platinum contact metal and gold bonding metal
- Dice the individual chips from the wafer
- Release the plates and springs from the substrate using hydrofluoric acid based wet etch

The glass wafer processing is as follows:

- Pattern and wet etch the indention for the electrostatic electrode
- Pattern by liftoff and deposit the Pt contact metal, the Au electrical lines, and the Au bond metal
- Dice the glass wafer into individual chips

The two chips are then aligned and bonded together using a flip-chip bonder.

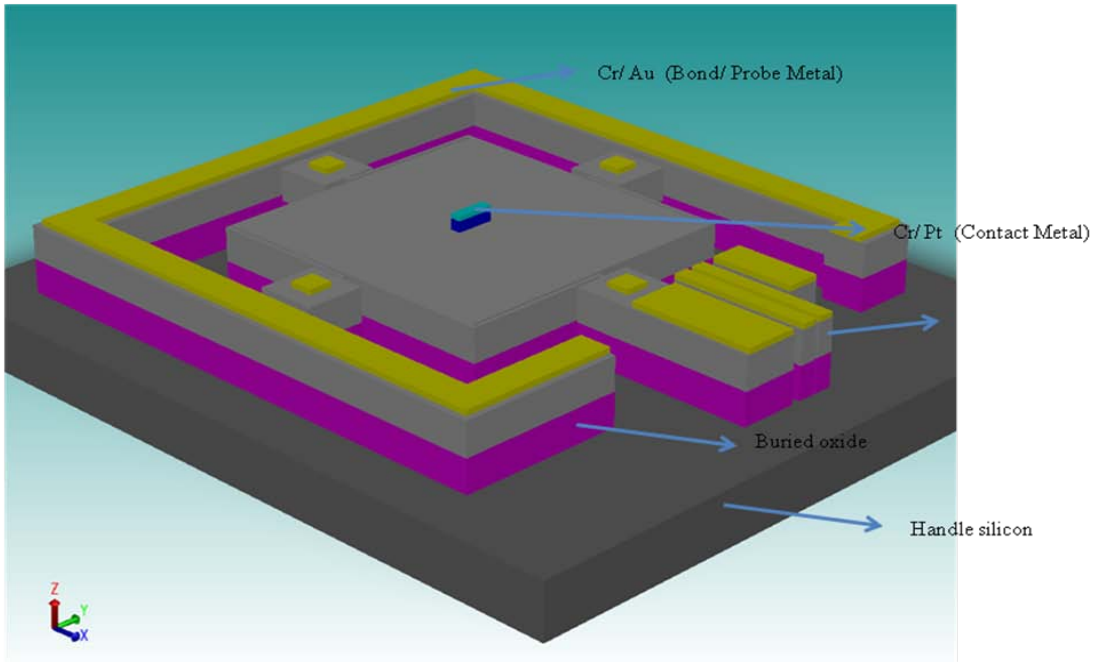


Figure 1: 3D solid model of the SOI wafer illustrating the 500 um x 500 um MEMS plate with contact and bond area. The plate can be electrostatically actuated towards the glass electrode after removal of the buried oxide layer under the plate.

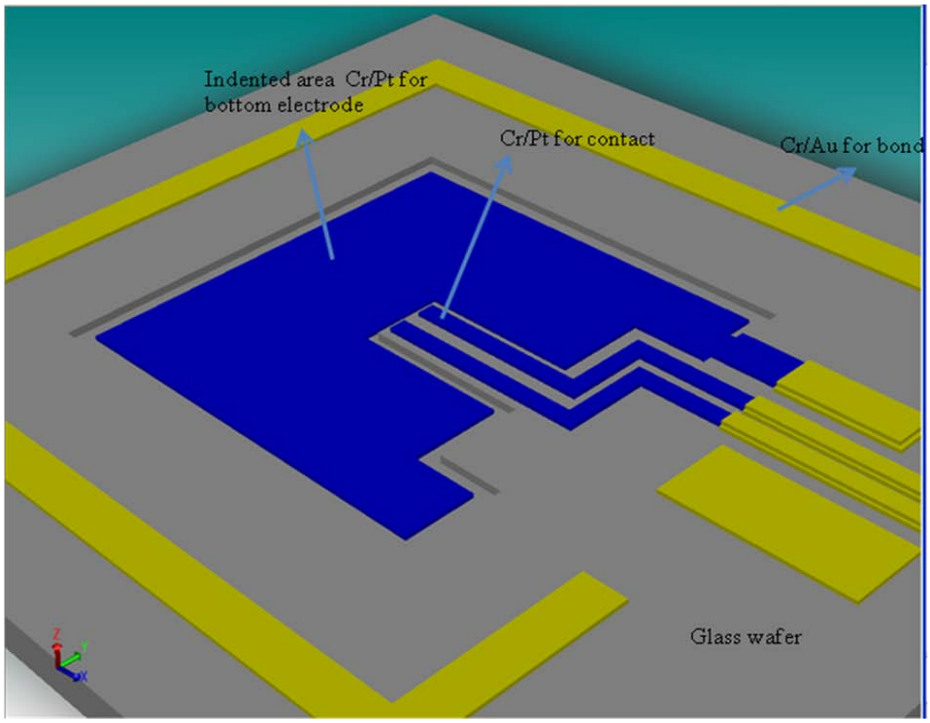


Figure 2: 3D solid model of the glass wafer illustrating the bottom electrode, contact and bond area. The glass wafer is bonded to the SOI wafer using Au-Au thermal compression bonding.

DIAMOND HEAT SPREADER OR HEAT SINK FOR HIGH POWER MEMS SWITCHES APPLICATIONS (TASK 1.3)

Contributors: Priscila Spagnol, Shinzo Onishi, Drew Hanser, John Bumgarner, Sunny Kedia

Deliverable: Prototype device fabricated on a thin-film diamond heat spreader layer and individual samples of diamond on Si or other suitable substrates for material evaluation.

Thermal conductivity measurement using the 3-ω method:

The issues addressed this month were:

- A new circuit configuration was implemented providing more accurate measurement by eliminating heater/sensor end effects in the measurement circuit that were not previously accounted for.
- A robust new heater/sensor wire pattern was transferred onto four substrates. The configuration of the measurement terminals in the new pattern enables improved electrical connection during measurement, which simplified measurements and let us acquire better quality data (improved repeatability, lower noise.)

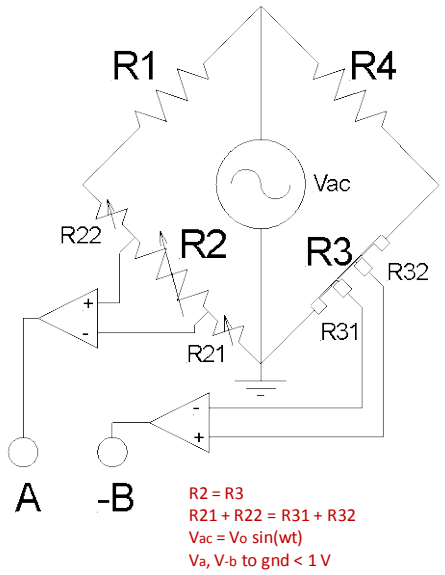
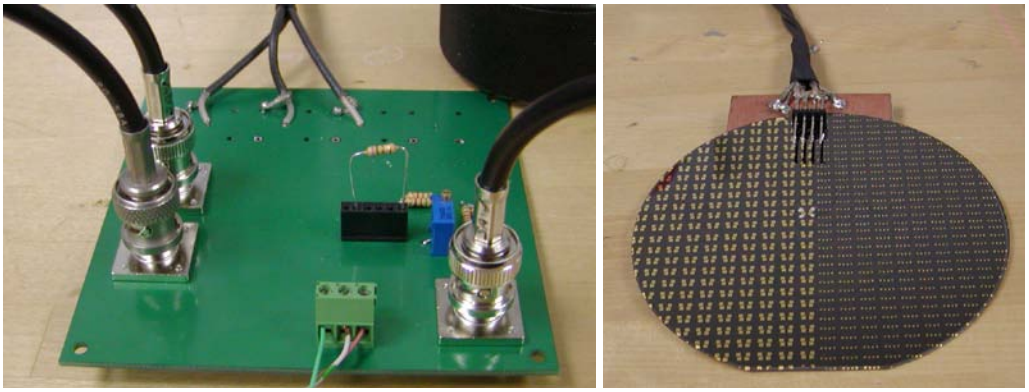


Figure 3: Schematic of the modified 4-terminal circuit used in the thermal conductivity measurements. The additions of resistors R21 and R22 improve the balance of the circuit and provide more accurate measurements.

The 4-terminal bridge circuit used for the thermal conductivity measurements is shown schematically in Figure 3. This circuit configuration enables us to extract the 3-ω voltage signal from the on-wafer sensor by comparing the signals from two precision operational amplifiers on both sides of the bridge circuit. Additional resistors in the circuit also allow the circuit to be better balanced.

To create the 4-terminal circuit, the existing PC board that was previously used for 2-terminal measurements was modified using jumper wires and components as shown in Figure 4 (a). The reconfigured circuit was used with the new heater/sensor patterns shown in Figure 4 (b). The output waveforms taken from the operational amplifiers are well balanced, as shown in Figure 5. The differential signal A(1) – B(2), shown as M1 in Figure 5, was analyzed with a lock-in amplifier and was used to determine the thermal conductivity of the different samples.

The results of thermal conductivity measurements using both the 2-terminal and the 4-terminal circuit configurations are shown in Table 1. Differences in the values of the thermal conductivity of the samples using the two circuit configurations are observed, as expected. We are continuing to evaluate the accuracy of the thermal conductivity measurements using the new circuit configuration by analyzing the 3-ω voltage signal across different frequency ranges.



(a) **(b)**

Figure 4: (a) The modified 4-terminal circuit board used to provide more accurate thermal conductivity measurements compared to the 2-terminal circuit; (b) the new heater/sensor design patterned on a polycrystalline diamond film on a silicon substrate.

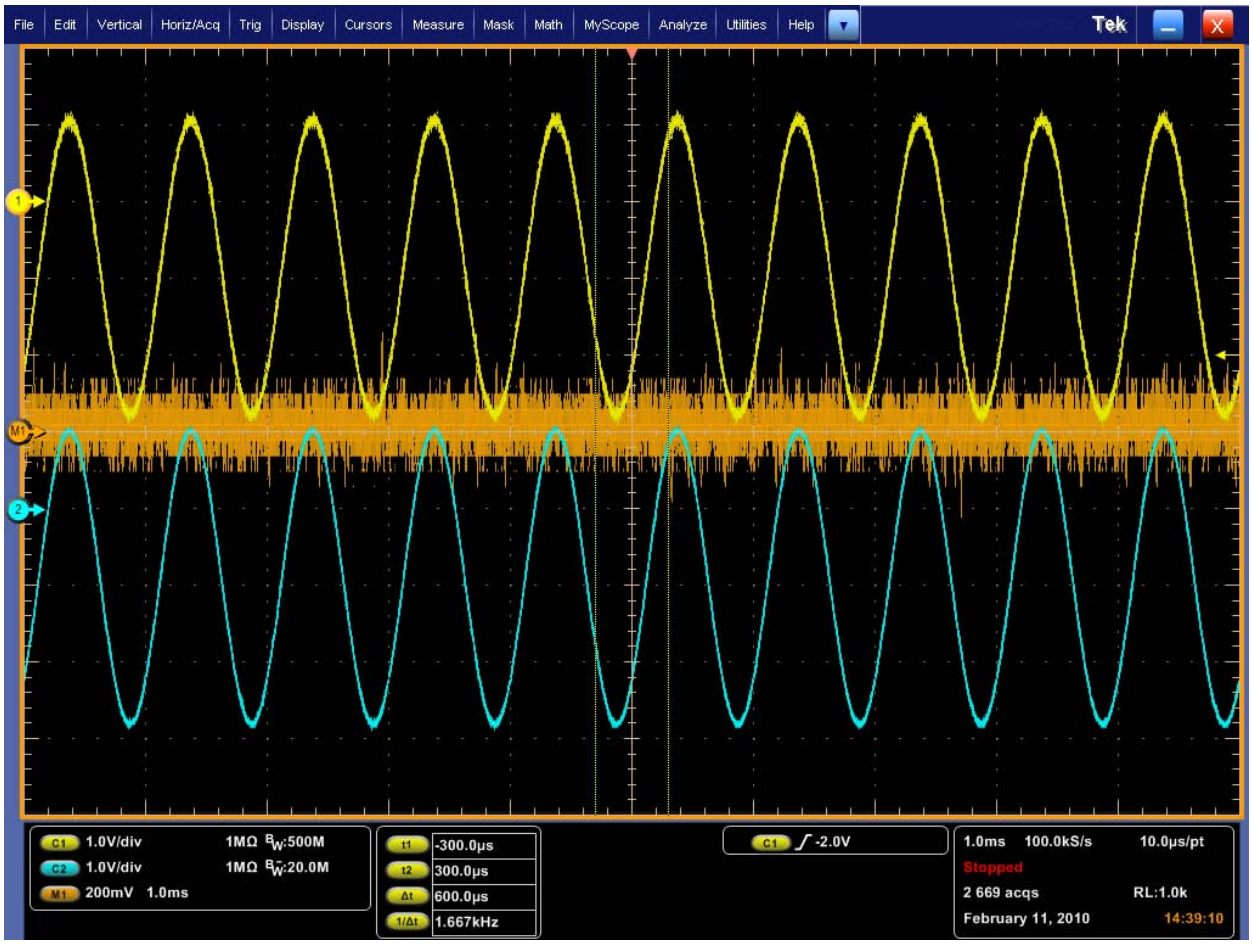


Figure 5: Waveforms A (1) and B (2) from the operational amplifiers in the 4-terminal circuit. The differential signal A – B (M1, orange trace) is analyzed using a lock-in amplifier to measure the 3-ω voltage signal, which is used to calculate the thermal conductivity.

Table 1: Thermal conductivity measurements made using the 2-terminal and 4-terminal circuit configurations. Differences are observed in the thermal conductivity values due to the differences in the measurement circuits and possible effects due to the frequency range of measurement.

Materials	Material/substrate Thickness [µm]	Thermal conductivity using 2 terminals [$W \cdot m^{-1} \cdot K^{-1}$]	Thermal conductivity using 4 terminals [$W \cdot m^{-1} \cdot K^{-1}$]
Polycrystalline diamond/Si	15/500	1236	869
Nano diamond/Si	1.72/3000	194	202
Nano diamond/Si	2.77/3000	Not measured	209
Nano diamond/Si	8.76/3000	Not measured	233
SiO_2/Si	0.05/500	132	148
Pyrex	500	7	15

Microcrystalline diamond freestanding wafers: This month, four thick microcrystalline diamond (MCD) films were grown on 2 inch silicon substrates. These films were grown on a buffer layer stack that consisted of a 2 µm nanocrystalline diamond layer deposited on a 6 µm thermal silicon oxide buffer layer.

The microwave power for the MCD films was varied from 2.7 to 3.3 kW for the different growth runs, which directly influences the substrate temperature, while all the other parameters were kept constant. The best growth results for the MCD films were observed at 2.9 kW and 3.0 kW. For these 2 runs, the growth rate was ~1.7 µm/h and neither cracked once the Si substrate was removed. The other two samples grown at 2.7 and 3.3 kW both cracked during the silicon substrate removal process.

POSITRON TRAPPING AND STORAGE (TASK 2)

Contributors: Ashish Chaudhary, Friso van Amerom, Tim Short

Deliverable: A minimum of four MEMS-based trap structures for RF trapping of electrons

Progress:

Fabrication

First prototype electron traps have been fabricated and are awaiting test setup assembly to be completed and electron generation and detection to be tested.

Test Setup

A test setup was designed, and most of the components have been assembled using Kimball Physics eV parts (Figure 6). To build a fast, switchable electron source, a UV light emitting diode (LED) (255 nm) was installed in front of a Burle Electro Optics micro channel plate (MCP). The MCP will be irradiated by UV light from the LED, thereby generating electrons. A high potential applied across the MCP will accelerate the electrons down the micro channels to cause a cascade effect, resulting in a relatively high electron output current (up to 10^5 electrons per photon). Two high-transparency nickel meshes (222 lines per inch) were installed on either side of the electron trap assembly to shield the electric field inside the trap from any perturbations from the adjacent high voltage components. A high-luminosity P-22 blue type phosphor screen was installed to detect the electrons ejected from the trap, and a high-transparency mesh was installed close to the phosphor screen to accelerate the electrons to the energy levels (>500 eV) to achieve good phosphor screen sensitivity. A silicon photomultiplier (SPM) was placed on the other side of the phosphor screen for detection of photons generated by the impinging electrons on the phosphor screen. A mu-metal shield was designed and fitted around the electron trap assembly to minimize the effect of any stray magnetic and electric fields that might be present in the vacuum housing.

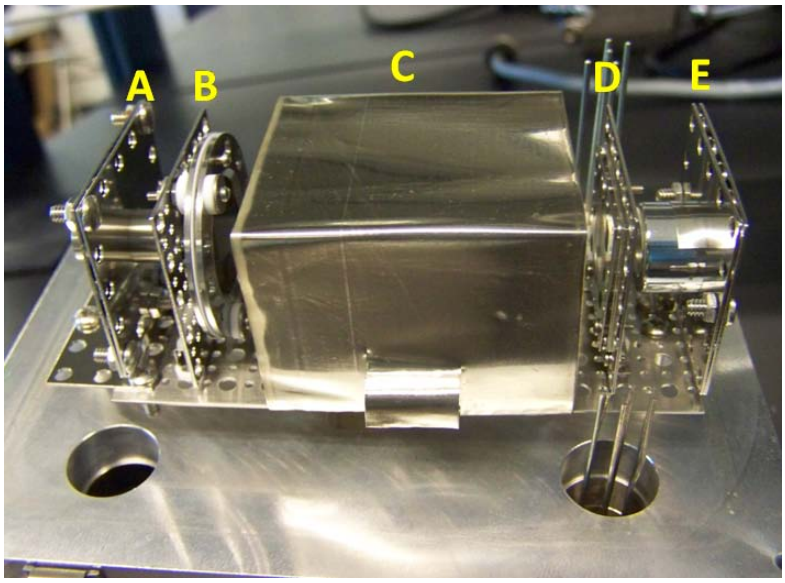


Figure 6: Electron trap test setup showing A: UV LED source; B: MCP; C: Mu-metal shield enclosing the electron trap assembly with nickel meshes on both ends; D: Phosphor screen with nickel mesh on the left; E: A tube casing in which the SPM will be installed.

Installation will be complete and electron trapping experimentation started in March, 2010.

OUTSTANDING ISSUES

SRI International has government furnished equipment (GFE) accountable to Contract W9113M-09-C-0135 with the Army (USAMDS/ARSTRAT). A request was submitted to the Army Contracting Officer requesting approval to use the GFE on a rent-free, non-interference basis on other US government programs SRI is supporting, including the Power MEMS contract. The Army Contracting Officer has requested ONR concurrence that ONR is agreeable with our plan to use the Army-supplied GFE to complete work on the ONR contract. A letter requesting a note from ONR was sent this month (1 February, 2010). The SRI KO is working with the ONR COTR to resolve questions regarding the equipment usage. Until the acceptance is granted, we will not be allowed to perform wafer processing on this project at SRI's Largo, FL facility.

Financial Status

R&D Status Report

Program Financial Status

15 July 2009 through 27 February 2010

Contract Item No.	Current Funding	Current Period Expenses	Cumulative Expenses	% Budget Complete
0001	$1,829,849	$64,469	$641,438	41%
Project Commitments		0	$263,886	
Total	$1,829,849	$64,469	$905,324	

Based on currently authorized work:

Is current funding sufficient for the current fiscal year (FY)? (Explain if NO) **Yes**

What is the next FY funding requirement at current anticipated levels **N/A** (**base fully funded)**